Notice of Allowability	Application No.	Applicant(s)	
	09/847,306	BU, LIN-KAI	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the application filed May 3, 2001*.

2. ☒ The allowed claim(s) is/are *1-6*.

3. ☒ The drawings filed on *03 May 2001* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 8/2/01
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Robert Gnuse on August 24, 2004.

The application has been amended as follows:

2. In the specification, insert the following after the "Background of the Invention" title:

This application claims priority to Taiwanese Application No. 90106145, filed March 15, 2001.

3. The title of the application is replaced by the following title:

High Bandwidth Low Power Differential Transmitter

4. The following claim listing replaces all prior versions and listings of claims in the application in their entirety:

1. ~~(a)~~ A data transmitter for receiving a single-ended binary input signal and converting the single-ended binary signal to a differential binary output signal, the data transmitter comprising:

(a) a first and a second conduction paths connected in parallel between a first and a second nodes;

(b) a first and a second switches connected in series in the first conduction path, wherein the first switch is located ~~near~~ closer to the first node, and the second switch is located ~~near~~ closer to the second node;

(c) a third and a fourth switches connected in series in the second conduction path, wherein the third switch is located ~~near~~ closer to the first node, and the fourth switch is located ~~near~~ closer to the second node;

(d) a source follower NMOS transistor ~~used as a source follower~~ having a drain connected to a voltage source, a gate connected to a first driving voltage, and a source connected to the first node, for providing current to the first and the second conduction paths via the first node; and

(e) a source follower PMOS transistor ~~used as a source follower~~ having a drain connected to ~~the~~ ground, a gate connected to a second driving voltage, a source connected to the second node for receiving current from the first and the second conduction paths via the second node;

wherein ~~the press control terminals~~ a control terminal of each of the first switch, the second switch, the third switch and the fourth switch are ~~respectively~~ each provided with one of the single-ended binary input signal or the ~~reverse direction~~ inverse signal thereof for cutting off the second and the third switches when the first and the fourth switches are turned on, and for cutting off the first and the fourth switches when the second and the third switches are turned on; the differential binary output signal ~~is~~

pulled out by a pair of output terminals, one of the output terminals is connected ~~to the connection area of~~ between the first and the second switches within the first conduction path, while the other output terminal is connected ~~to the connection area of~~ between the third and the fourth switches within the second conduction path.

2. A data transmitter as set forth in claim 1, wherein the first and the third switches are PMOS transistor switches, and the second and the fourth switches are NMOS transistor switches, and the first driving voltage is generated by ~~the~~ a first driving voltage output circuit, and the second driving voltage is generated by ~~the~~ a second driving voltage output circuit, wherein the first driving voltage output circuit ~~comprising~~ comprises:

(a) a first fixed current source having ~~a bottom~~ an output terminal connected to ~~the~~ ground;

(b) a first NMOS transistor and a first PMOS transistor, wherein the sources of both the transistors are connected, the drain of the first NMOS transistor is connected to the voltage source, the gate of the first NMOS transistor is connected to the gate of the source follower NMOS transistor ~~that is used as the source follower~~, the drain of the first PMOS transistor is connected to ~~the top~~ an input terminal of the first fixed current source, and the gate of the first PMOS transistor is connected to ~~the~~ ground; and

(c) a first comparator having a positive input terminal connected to a first reference voltage, a negative input terminal connected to the ~~top~~ input terminal of the first fixed

current source, and ~~the~~ an output terminal being connected to the gate of the first NMOS transistor; and

wherein the second driving voltage output circuit ~~comprising~~ comprises:

(d) a second fixed current source having ~~a top~~ an input terminal connected to the ~~ground~~ voltage source;

(e) a second NMOS transistor and a second PMOS transistor, wherein the sources of both the transistors are connected, ~~and~~ the drain of the second PMOS transistor is connected to ~~the~~ ground; the gate of the second PMOS transistor is connected to the gate of the source follower PMOS transistor ~~that is used as the source follower~~; the drain of the second NMOS transistor is connected to ~~the bottom~~ an output terminal of the second fixed current source, and the gate of the second NMOS transistor is connected to the voltage source; and

(f) a second comparator having a positive input terminal for receiving a second reference voltage, and a negative input terminal connected to the ~~bottom~~ output terminal of the second fixed current source, and an output terminal connected to the gate of the second PMOS transistor.

3. A data transmitter as set forth in claim 1, wherein the first and the third switches are PMOS transistor switches, and the second and the fourth switches are NMOS transistor switches, and the first driving voltage is generated by ~~the~~ a first driving voltage output circuit, and the second driving voltage is generated by ~~the~~ a second driving voltage output circuit, wherein the first driving voltage output circuit ~~further~~ comprises:

(a) a first fixed current source having ~~a top~~ an input terminal connected to ~~a~~ the voltage source;

(b) a first resistor having a first terminal connected to ~~the~~ ground; and

(c) a first NMOS transistor and a first PMOS transistor, wherein the sources of both the transistors are connected, the drain of the first NMOS transistor is connected to the gate of the first NMOS transistor~~,~~ and ~~the drain is connected in parallel at the bottom~~ an output terminal of the first fixed current source, the gate of the first NMOS transistor is connected to the gate of the source follower NMOS transistor ~~that is used as the source follower~~, the drain of the first PMOS transistor is connected to ~~the~~ a second terminal of the resistor, and the gate of the first PMOS transistor is connected to ~~the~~ ground; and

wherein the second driving voltage output circuit ~~further~~ comprises:

(d) a second fixed current source having ~~a bottom~~ an output terminal connected to ~~the~~ ground;

(e) a second resistor having a first terminal connected to the voltage source; and

(f) a second NMOS transistor and a second PMOS transistor, wherein the sources of both the transistors are connected, the drain of the second PMOS transistor is connected to the gate of the second PMOS transistor~~,~~ and ~~the drain is connected in parallel at the top~~ an input terminal of the second fixed current source, the gate of the second PMOS transistor is connected to the gate of the source follower PMOS transistor ~~that is used as the source follower~~, the drain of the second ~~PMOS~~ NMOS

transistor is connected to ~~the~~ a second terminal of the resistor, and the gate of the second NMOS transistor is connected to the voltage source.

4. A data transmitter for receiving a single-ended binary input signal and converting the single-ended binary signal to a differential binary output signal, the data transmitter comprising:

(a) a first and a second conduction paths connected in parallel between a first and a second nodes;

(b) a first and a second switches connected in series in the first conduction path, wherein the first switch is located ~~near~~ closer to the first node, and the second switch is located ~~near~~ closer to the second node.

(c) a third and a fourth switches connected in series in the second conduction path, wherein the third switch is located ~~near~~ closer to the first node, and the fourth switch is located ~~near~~ closer to the second node;

(d) an emitter follower npn transistor ~~that is used as an emitter follower~~ having a collector connected to a voltage source, a base connected to a first driving voltage, an emitter connected to the first node, for providing current to the first and the second conduction paths via the first node; and

(e) an emitter follower pnp transistor ~~that is used as an emitter follower~~ having a collector connected to ~~the~~ ground, a base connected to ~~the~~ a second driving voltage, an emitter connected to ~~a~~ the second node for receiving current from the first and the second conduction paths via the second node;

wherein ~~the press-control terminals~~ a control terminal of each of the first switch, the second switch, the third switch and the fourth switch are ~~respectively~~ each provided with one of the single-ended binary input signal or the ~~reverse direction~~ inverse signal thereof for cutting off the second and the third switches when the first and the fourth switches are turned on, and for cutting off the first and the fourth switches when the second and the third switches are turned on; the differential binary output signal ~~is~~ pulled out by a pair of output terminals, wherein one of the output terminals is connected ~~to the connection area of~~ between the first and the second switches within the first conduction path, and the other output terminal is connected ~~to the connection area of~~ between the third and the fourth switches within the second conduction path.

5. A data transmitter as set forth in claim 4, wherein the first and the third switches are pnp transistor switches, and the second and the fourth switches are npn transistor switches, and the first driving voltage is generated by ~~the~~ a first driving voltage output circuit, and the second driving voltage is generated by ~~the~~ a second driving voltage output circuit, wherein the first driving voltage output circuit comprises:

(a) a first fixed current source having ~~a bottom~~ an output terminal connected to ~~the~~ ground;

(b) a first npn transistor and a first pnp transistor, wherein the emitters of both the transistors are connected, the collector of the first npn transistor is connected to the voltage source, the base of the first npn transistor is connected to the base of the emitter follower npn ~~that is used as the emitter follower~~ transistor, the collector of the

first pnp transistor is connected to ~~the top~~ an input terminal of the first fixed current source, and the base of the first pnp transistor is connected to ~~the~~ ground; and

(c) a first comparator having a positive input terminal connected to a first reference voltage, a negative input terminal connected to the ~~top~~ input terminal of the first fixed current source, and an output terminal connected to the base of the first npn transistor; and

wherein the second driving voltage output circuit comprises:

(d) a second fixed current source having ~~a top~~ an input terminal connected to the ~~ground~~ voltage source;

(e) a second npn transistor and a second pnp transistor, wherein the emitters of both the transistors are connected, the collector of the second pnp transistor is connected to ~~the~~ ground, ~~and~~ the base of the second pnp transistor is connected to the base of the emitter follower pnp transistor ~~that is used as the emitter follower~~, the collector of the second npn transistor is connected to ~~the bottom~~ an output terminal of the second fixed current source, and the base of the second npn transistor is connected to the voltage source; and

(f) a second comparator having a positive input terminal for receiving a second reference voltage, a negative input terminal connected to the ~~bottom~~ output terminal of the second fixed current source, and an output terminal connected to the base of the second pnp transistor.

6. A data transmitter as set forth in claim 4, wherein the first and the third switches are pnp transistor switches, and the second and the fourth switches are npn transistor switches, and the first driving voltage is generated by ~~the~~ a first driving voltage output circuit, and the second driving voltage is generated by ~~the~~ a second driving voltage output circuit, wherein the first driving voltage output circuit comprises:

(a) a first fixed current source having ~~a top~~ an input terminal connected to ~~a~~ the voltage source;

(b) a first resistor having a first terminal connected to ~~the~~ ground; and

(c) a first npn transistor and a first pnp transistor, wherein the emitters of both the transistors are connected, the collector of the first npn transistor is connected to the base of the first npn transistor~~,~~ and ~~the collector is connected in parallel at the bottom~~ an output terminal of the first fixed current source, the base of the first npn transistor is connected to the base of the emitter follower npn transistor ~~that is used as the emitter follower~~, the collector of the first pnp transistor is connected to ~~the~~ a second terminal of the resistor, and the base of the first pnp transistor is connected to ~~the~~ ground; and

wherein the second driving voltage output circuit comprises:

(d) a second fixed current source having ~~a bottom~~ an output terminal connected to ~~the~~ ground;

(e) a second resistor having a first terminal connected to the voltage source; and

(f) a second npn transistor and a second pnp transistor, wherein the emitters of both the transistor are connected, the collector of the second pnp transistor is connected

to the base of the second pnp transistor~~,~~ and ~~the collector is connected in parallel at the top~~ an input terminal of the second fixed current source, the base of the second pnp transistor is connected to the base of the emitter follower pnp transistor ~~that is used as the emitter follower~~, the collector of the second npn transistor is connected to ~~the~~ a second terminal of the resistor, and the base of the second npn transistor is connected to the voltage source.

Allowable Subject Matter

5. Claims 1-6 are allowed.

6. The following is an examiner's statement of reasons for allowance:

Claims 1-6 are found to be allowable over the prior art of record because they are distinguished from the prior by the configuration of the source follower NMOS and PMOS transistors (claim 1) and the emitter follower npn and pnp transistors (claim 2). Figure 1 of the instant application illustrates that the NMOS transistor N1 is between the node A and a voltage source while the PMOS transistor P1 is between the node B and ground. The prior art of record specifies an alternative configuration wherein a PMOS transistor would equivalently be placed between node A and a voltage source while an NMOS transistor would equivalently be place between node B and gound (for instance, see US. Pat. No. 5767699 to Bosnyak et al). Further, the variations between the instant application and that of the prior art are not found to be obvious.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art is cited to show the current state of the art with respect to differential transmitters.

U.S. Pat. No. 6201405 to Hedberg.

U.S. Pat. No. 6222388 to Bridgewater, Jr.

U.S. Pat. No. 5285477 to Leonowich.

U.S. Pat. No. 5767699 to Bosnyak et al.

U.S. Pat. No. 5959472 to Nagamatsu et al.

U.S. Pat. No. 6288581 to Wong.

U.S. Pat. No. 6111431 to Estrada.

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